LSF010XEVM-001

This document is the user's guide for the LSF010XEVM-001 Evaluation Module (EVM). The EVM allows for evaluation of the different ways that the LSF devices can be used to translate voltages between 1 V and 5.5 V.

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1 About This Manual

This user's guide describes the LSF010XEVM-001. This guide contains an introduction, setup instructions, the EVM schematic, top and bottom printed-circuit-board (PCB) layouts, and a bill of materials (BOM).

2 Information About Cautions and Warnings

The information in a caution or a warning is provided for your protection. Read each caution and warning carefully.

CAUTION

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see the *Electrostatic Discharge* (ESD) application note (SSYA008).

3 Items Required for Operation

- Volt meter
- Oscilloscope
- Square wave signal source

4 Introduction

The LSF010XEVM-001 is an EVM board that contains 3 LSF voltage clamp translators: 1bit, 2-bit and 8 bit. These translators are bi-directional and do not require a control pin. They can except voltages up to 5.5 V on the inputs and the output will be equal to the VrefA voltage. Once the output reaches the VrefA level it can then be pulled to any other level between VrefA and 5.5 V. When using multi-bit LSF devices you can have many different levels of voltage translation on the same part. They can translate at medium to high speeds up to 100 MHz and cover these common voltage nodes and anything in between (1 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V). These devices act like a switch when the input is between GND and Vref A and will have FET switch type characteristics such as speeds up to 200 MHz when translating down. Then the I/Os can be pulled up to any voltage between VrefA and 5.5 V. The maximum speed will then be limited by the size of the pull-up resistor and speeds up to 100 MHz can be achieved when translating up.

The LSF010XEVM-001 EVM allows simplified evaluation and prototyping without the need for full board development. This EVM provides peripheral header style pads for probing and signal connection to each device pin and can be plugged into any prototype board with DIP header spacing. The boards are scored so they can easily be broken apart.
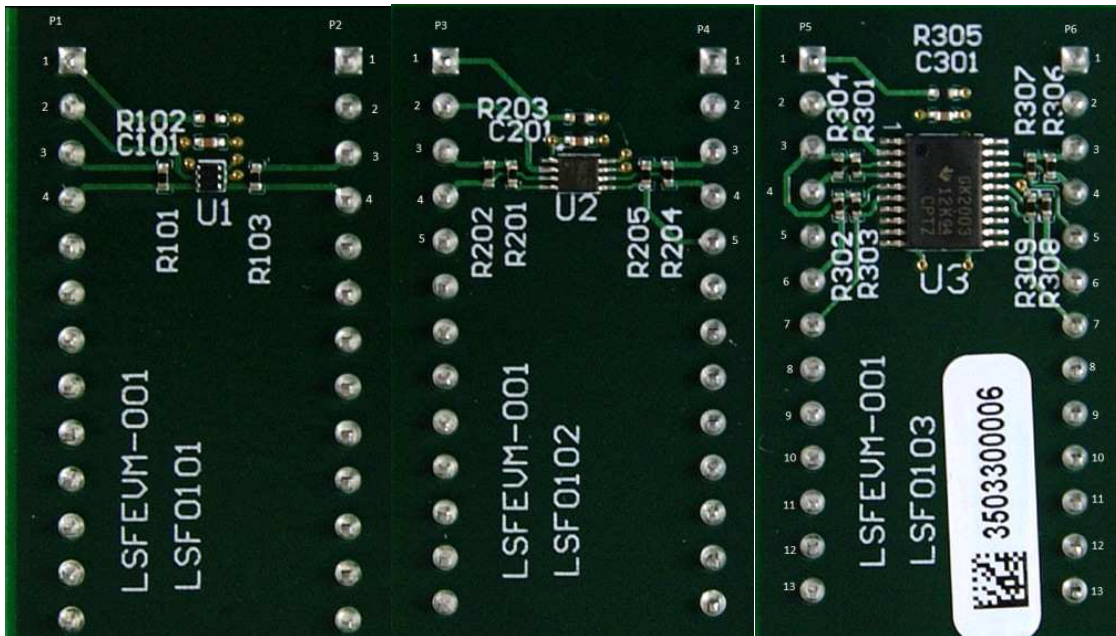
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Figure 1. EVM Board

PW Package (TOP VIEW)

DCT or DCU Package (TOP VIEW)

DRY Package (TOP VIEW)
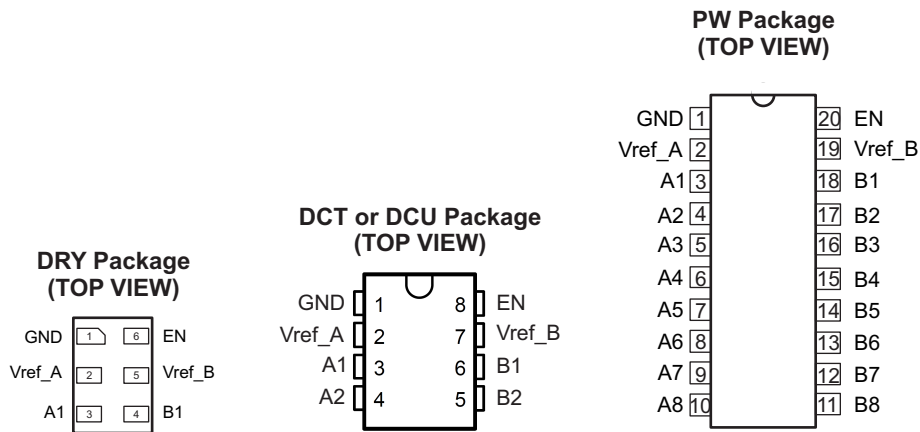
Table 1. Device and Package Configurations

LSFEVM001	ICs	Package
U1	LSF0101DRY	SON
U2	LSF0102DCU	US8
U3	LSF0108PW	TSSOP

5   Setup

This section describes the setup and connections of the EVM boards and describes how to set up the boards for voltage translations in either up or down direction.

5.1 *General Rules for Good Signal Integrity*

Ensure that Vref_A , Vref_B and GND are all connected and configured properly. There should be a bypass capacitor on Vref_B (0.1 µF). When connecting signals, minimize the connection length and keep GND leads short when probing. This will ensure minimal capacitive, resistive and inductive loading caused by the connection and connector. For more device information please see the LSF0101, LSF0102, and LSF0108 device datasheet.

5.1.1 VCC and GND Connections

Vref_B is considered VCC or device power. It will need to be 1V greater than Vref_A. Vref_A will be the lowest voltage that the part can translate down to.

GND is connected to pin 1 of P2 (LSF0101), Pin 1 of P4 (LSF0102), and Pin 1 of P6 (LSF0108). See connector pin locations in Figure 1 .

5.1.2 Translation Connections

On each board there will be a VAPU and a VBPU connection. These are the pull-up voltages that correspond to the voltage being translated. These pull-up voltages must be between or equal to VrefA and VrefB.

Some of the I/O pins on the LSF0108 will not have pull-up resistors. This will allow the use of different pull-up resistor values and voltages on the A or B side. The A and B pins can be pulled to different levels on each pin demonstrating that the part can translate many different voltage levels at the same time. (The pull-up resistors installed on the boards are 301 Ω)

The following are examples of how the parts can be set up:

Each of these tests can be performed on any of the boards.

NOTE: The LSF0101 and LSF0102 have all their pins connected to pull-up resistors on the EVM. The A and B pins without pull-up resistors on the LSF0108 are the only pins that can be pulled down.

Test examples
There can be multiple types of tests performed on each board. The drawing shows A as the input and B as the output; however, it can work either direction. The output on Aside or Bside will be limited to VrefA for a high level. Either side can then be pulled to any level between VrefA and 5.5 V. This allows up translation, down translation or any combination. The signals can go in both directions without the need for a direction pin.

Example 1 no pull-up
With no pull-up on either side (don't connect VAPU or VBPU), you will be able to translate down to VrefA going either direction. The input can be 0 V to 5.5 V and the output will be 0 V to VrefA. Either Apins or Bpins can be the input. This method can be used for down translation.

Example 2 with pull-up
By connecting VAPU or VBPU, you can pull the A or B side to any level between VrefA and 5.5 V. This method can be used for up translation. By connecting the outputs to multiple pull-up levels you are able to translate to a variety of different voltage nodes using a single part. Testing the part using multiple pull-up voltages can only be done on the LSF0108. The first four I/O's will be tied to the same pull-up voltage on the EVM. (VAPU or VBPU) The remaining four I/O's can be connected to external pullp resistors and different pull-up voltages.

Example 3 with pull-down
A pull-down to GND can also be used which will give the output value of VreA. This is sometime used to help with noise. If VREFA is the voltage that you are translating to then the pull-up can be tied to VREFA for another way to reduce noise.

Example 4 with open drain part (Figure 3)

This configuration allows you to control the input level with Vref. Using an open drain part on the input side will allow VrefA to control the input level. VBPU will control the output level of the LSF. Do not connect anything to VAPU. You can put in a 0 V to 5 V signal into the open drain part, a 2 V signal on Vref, and a 3.3 V signal on VBPU.

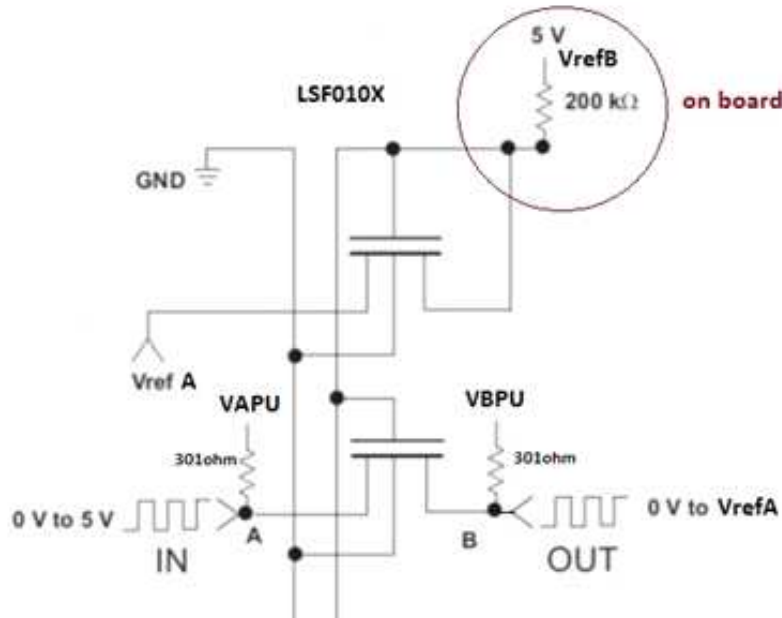This will then translate from 5 V to 2 V on Abus and then to 3.3 V on B bus.

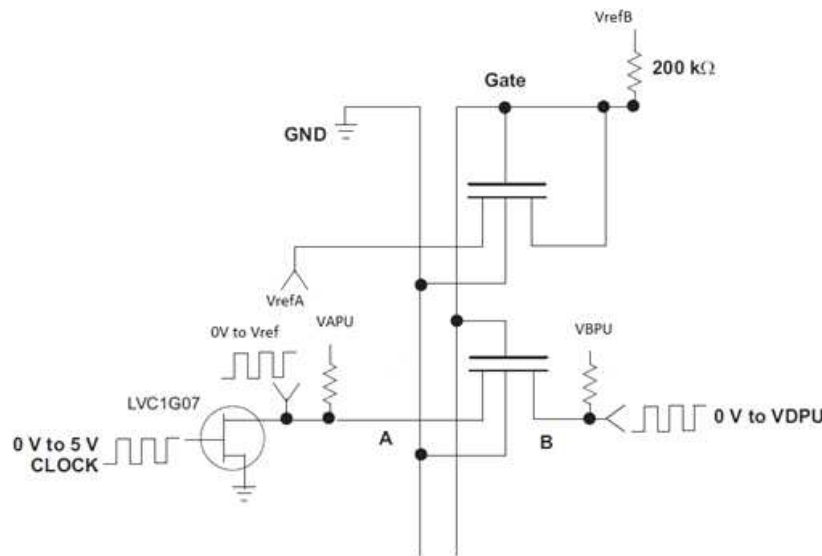**Figure 2. Pull-up Resistors on VAPU and VBPU**

Figure 3. Open Collector Input Control Circuit

6 Schematic

The circuit diagrams below show the schematics for the LSF010XEVM-001:

6.1 Board Schematics and Pin Layout
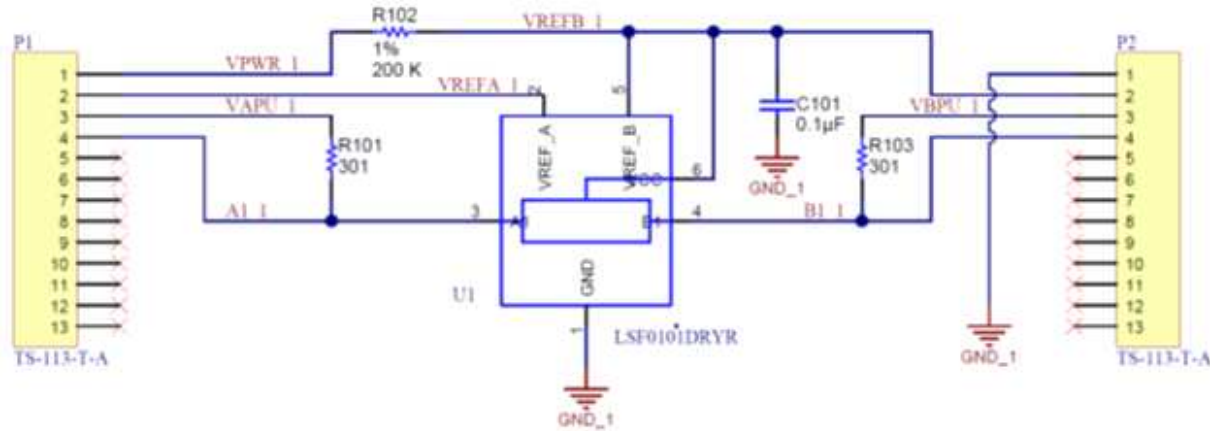
Figure 4. LSF0101 Schematic

Table 2. LSF0101

P1	Pin Out	P2	Pin Out
1	Power pin	1	GND
2	Vref_A	2	Vref_B Power pin
3	VAPU A side pull-up	3	VBPU B side pull-up
4	A1 signal	4	B1 signal
5	NC	5	NC
6	NC	6	NC
7	NC	7	NC
8	NC	8	NC
9	NC	9	NC
10	NC	10	NC
11	NC	11	NC
12	NC	12	NC
13	NC	13	NC
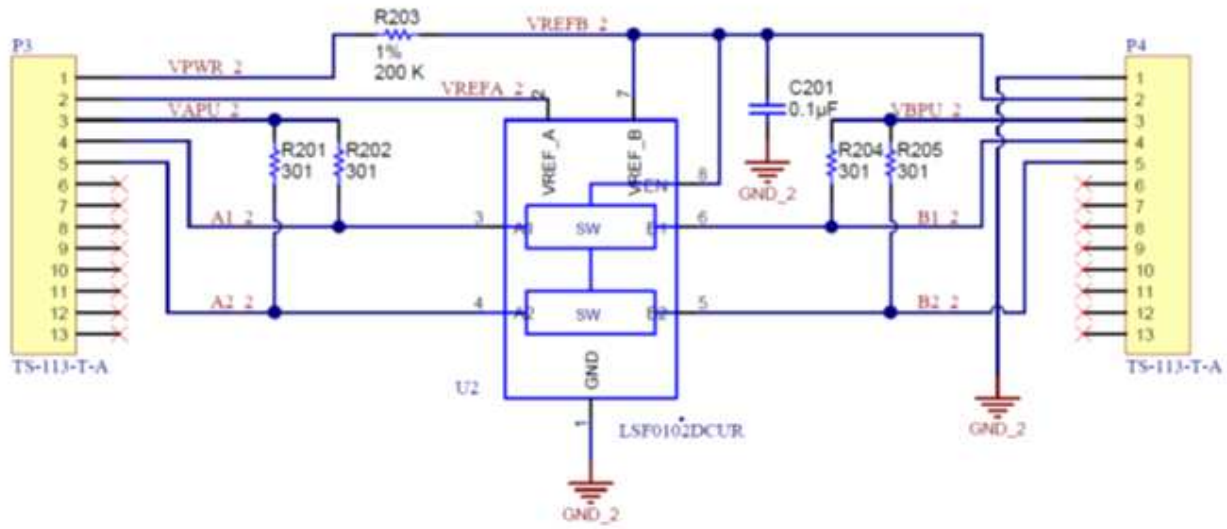
Figure 5. LSF0102 Schematic

Table 3. LSF0102

P3	Pin out	P4	
1	Pwr-Vref_B	1	GND
2	Vref_A	2	Vref_B Power pin
3	VAPU A side pull-up	3	VBPU B side pull-up
4	A1 signal	4	B1 signal
5	A2 signal	5	B2 signal
6	NC	6	NC
7	NC	7	NC
8	NC	8	NC
9	NC	9	NC
10	NC	10	NC
11	NC	11	NC
12	NC	12	NC
13	NC	13	NC
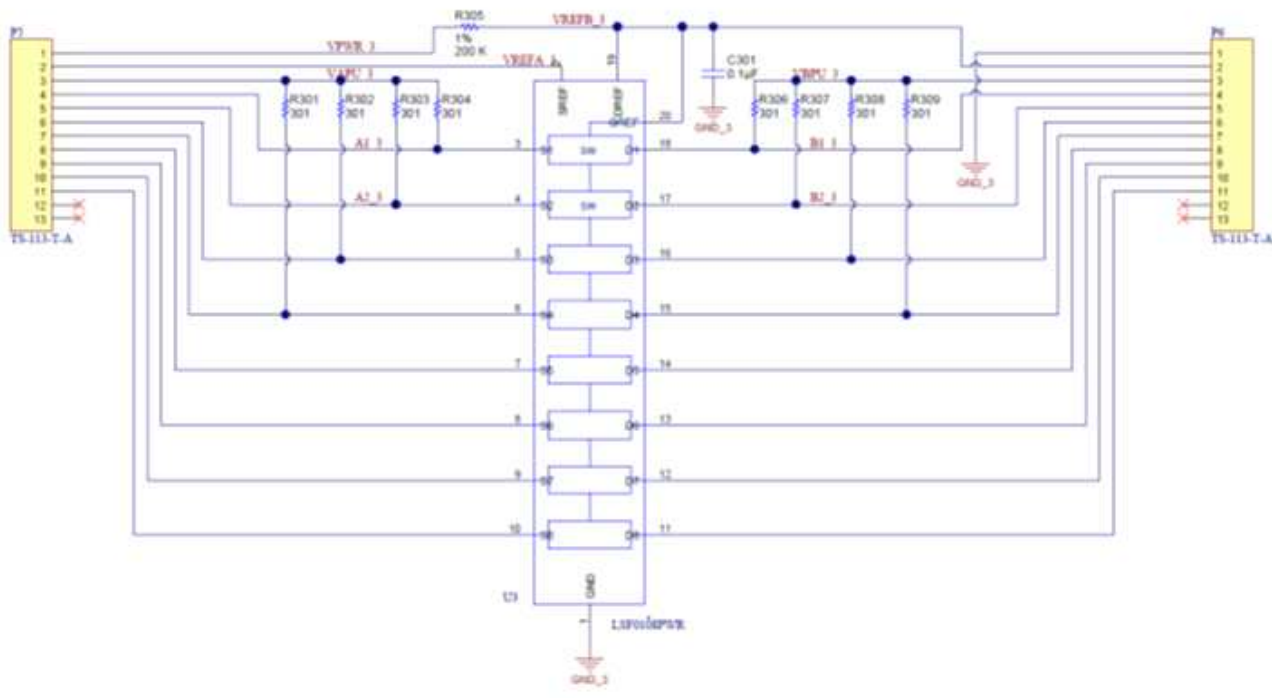
Figure 6. LSF0108 Schematic

Table 4. LSF0108

P5	Pin Out	P6	Pin Out
1	Pwr-Vref_B	1	GND
2	Vref_A	2	Vref_B Power pin
3	VAPU A side pull-up	3	VBPU B side pull-up
4	A1 signal	4	B1 signal
5	A2 signal (Not connected)[1]	5	B2 signal
6	A3 signal	6	B3 signal
7	A4 signal	7	B4 signal
8	A5 signal	8	A5 signal
9	A6 signal	9	A6 signal
10	A7 signal	10	A7 signal
11	A8 signal	11	A8 signal
12	NC	12	NC
13	NC	13	NC

[1]   Note pin 5 on P5 of the LSF0108 board is not connected.

7   B Board Layout

Figure 7 and Figure 8 illustrate the PCB layout.
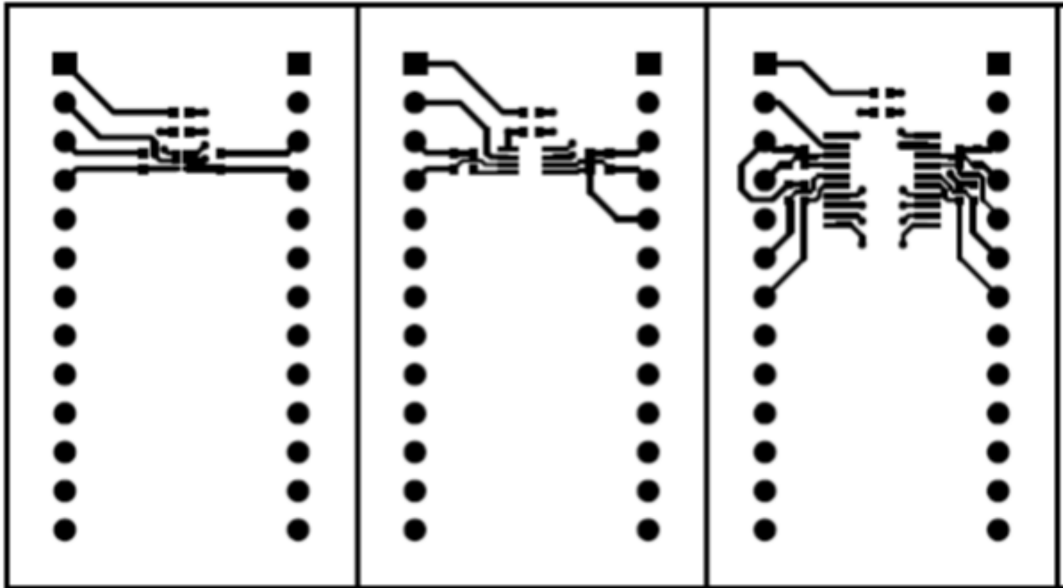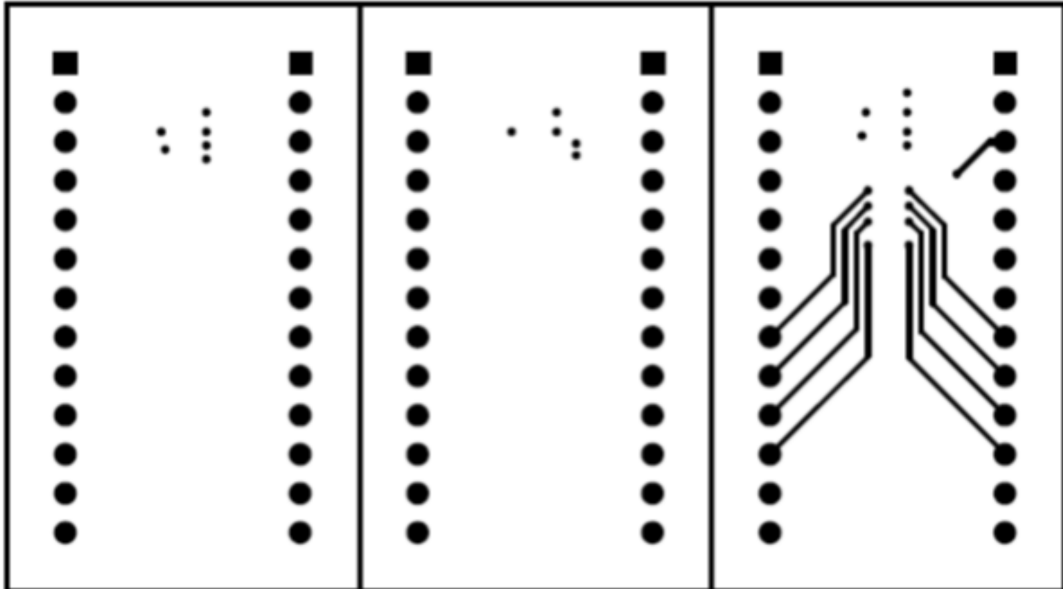

Figure 7. PCB Layer 1 (Top Layer)

Figure 8. PCB (Bottom Layer)

8　Bill of Materials (BOM)

Table 5 lists the BOM for the LSF EVM.

Table 5. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C101, C201, C301	3	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, C0G/NP0, 0402	0402	C1005X7R1H104K	TDK
P1, P2, P3, P4, P5, P6	6		Header, 13-Pin		TS-113-T-A	Samtec
R101, R103, R201, R202, R204, R205, R301, R302, R303, R304, R306, R307, R308, R309	14	301	RES, 301 ohm, 1%, 0.063W, 0402	0402	CRCW0402301RFKED	Vishay-Dale
R102, R203, R305	3	200 K	RESISTOR, 0402, 200K, 1%	0402	CRCW0402200KFKED	Vishay-Dale
U1	1	LSF0101DRYR	IC TRANSLATOR BIDIR 6SON		LSF0101DRYR	Texas Instruments
U2	1	LSF0102DCUR	IC LEVEL TRANSLATOR BIDIR US8		LSF0102DCUR	Texas Instruments
U3	1	LSF0108PWR	IC LEVEL TRANSLATOR BIDIR		LSF0108PWR	Texas Instruments

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